First Named Inventor	Scott Derner
Serial No.	10/017,658
Filing Date	December 12, 2002
Group Art Unit	2818
Examiner Name	Tan Nguyen
Facsimile No.	703-308-7724
Attorney Docket No.	400.105US01

FACSIMILE TRANSMITTAL TO USPTO

Title: HALF DENSITY ROM EMBEDDED DRAM

Total Pages: 7 (including transmittal sheet)

Commissioner for Patents
Washington, D.C. 20231

Enclosures

The following documents are enclosed:

FAX RECEIVED

X An Amendment and Response to Office Action of January 15, 2003 (6 pgs.).

APR 1 5 2003

TECHNOLOGY CENTER 2800

CUSTOMER NUMBER: 27073

PLEASE CHARGE ANY ADDITIONAL FEES OR CREDIT ANY OVERPAYMENTS TO DEPOSIT ACCOUNT 501373

Submitted By

Name	Daniel J. Polglaze	Reg. No.	39.801	Telephone	(612) 312-2203
Signature	Daniel J. Polglaze			Date	April 15, 2003

Attorneys for Applicant
Leffert Jay and Polglaze, P.A.
P.O. Box 581009
Minneapolis, MN 55458-10009
T: 612-312-2200
F: 612-312-2250

Certificate of Transmission

I certify that this paper, and the above-identified documents, are being transmitted by facsimile to Group 2818 at the United States Patent and Trademark Office on April 15, 2003.

Name	Susan W. Donovan	Signature	Susan W. Donovan

S/N 10/017,658

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Scott Derner
Serial No.: 10/017,658
Filed: December 12, 2001
Title: HALF DENSITY ROM EMBEDDED DRAM

Examiner: Tan Nguyen
Group Art Unit: 2818
Atty. Docket No.: 400.105US01

8/B
4-18-03

AMENDMENT AND RESPONSE

Commissioner for Patents
Washington, D.C. 20231

In response to the Office Action dated January 15, 2003, please amend the above-identified patent application as follows:

IN THE CLAIMS

1. (Original) A memory device comprising:
a read only memory (ROM) cell hard programmed to a first data state;
a dynamic memory cell; and
access circuitry to couple the ROM cell and the dynamic memory cell to differential digit lines.

2. (Original) The memory device of claim 1 wherein the access circuitry comprises:
a first transistor coupled between the ROM cell and a first digit line; and
a second transistor coupled between the dynamic memory cell and a second digit line, wherein gate connections of the first and second transistors are coupled to different word lines.

3. (Original) The memory device of claim 1 wherein the ROM cell is hard programmed to Vcc.

4. (Original) The memory device of claim 1 wherein the ROM cell is hard programmed to Vss.